LABORATORY III : Operational Amplifiers

A. Objective

In this week's lab we will investigate several circuits in order to understand the utility as well as the limitations of real-world op-amps. Try to view this lab not only as a learning experience about op-amps, but also as a practice exercise in making precise measurements with your oscilloscope. Think hard about the procedure you are being asked to carry out and what function is served by each of the steps.

B. Reading

- R. E. Simpson *Introductory Electronics for Scientists and Engineers* (Prentice-Hall, Englewood Cliffs, 1987), Chap. 9 (especially Sections 9.1, 9.4, 9.6 - 9.8).

C. Lab Exercises

In the exercises below, use an LF411 op-amp. The low offsets, high speed and low cost of this device make it an excellent choice for general-purpose applications. The pin diagram for the LF411 is shown below . The 741 op-amp, which has the same pin diagram, was the industry-standard in times past.

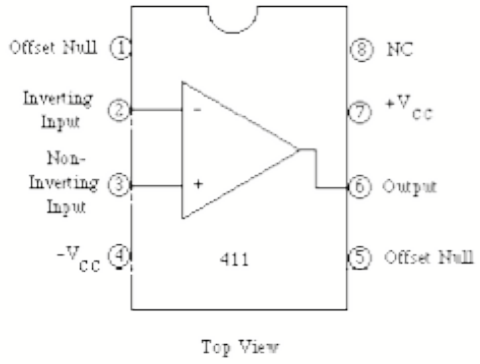


Figure 1: LF 411 op-amp

1. Measurement of Slew Rate

(a) To measure the LF411 slew rate, use the unity-gain voltage follower circuit shown below in Fig. 2. Drive the input with a square wave. Using two channels of your oscilloscope, simultaneously observe the input square-wave and the op-amp output. Measure the slew rate by observing the slope of the output transitions. Are rising and falling edges equally distorted? See what happens as the input amplitude is varied. Compare your measurements with the 411 specifications given on the attached sheet. If you are interested, repeat your measurements using a 741 op-amp; the pin connections are the same as for the 411. You will find that the 741 is much slower than the 411.

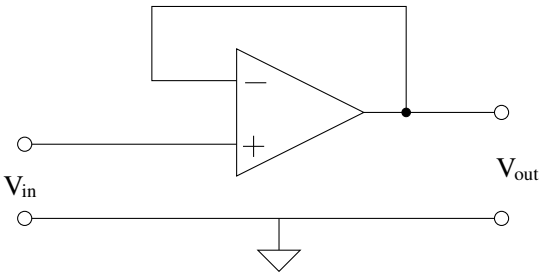


Figure 2: Unity gain follower circuit for measuring the slew rate

2. Measurement of Offset Voltage

(a) Measure the offset voltage using the amplifier itself to amplify the offset voltage to measurable values. For example, if the op-amp has an input offset voltage V_{os} and a gain of 1000 (as shown in Fig. 3), then $V_{out} = 1000V_{os}$. Compare your measured offset voltage with the 411 specifications found on the attached sheet.

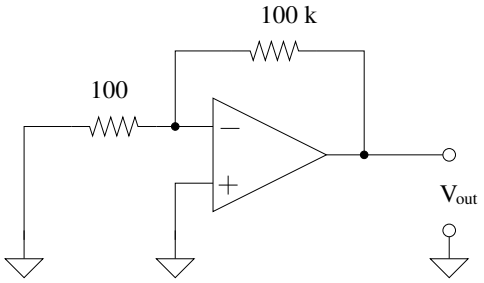


Figure 3: Inverting amplifier for testing the voltage offset.

(b) Trim the offset voltage to zero using the circuit shown in the spec sheet's *Typical Connection* diagram (also Figure 9.19 b in Simpson) and demonstrate that, by adjusting it properly, V_{os} can be eliminated (i.e., made zero). Make certain that you check that your potentiometer (=variable resistor) is functioning properly by testing it with an ohmmeter. In some cases a smaller range potentiometer has done a better job of trimming. Ensure that the negative 15 V is connected to the middle post of the potentiometer.

3. What limits the performance: the gain bandwidth product or the slew rate ?

As you know, both the finite gain-bandwidth product and the finite slew rate can lead to a finite rise-time and an op-amp gain that decreases with increasing frequency. In this measurement you are asked to explore this.

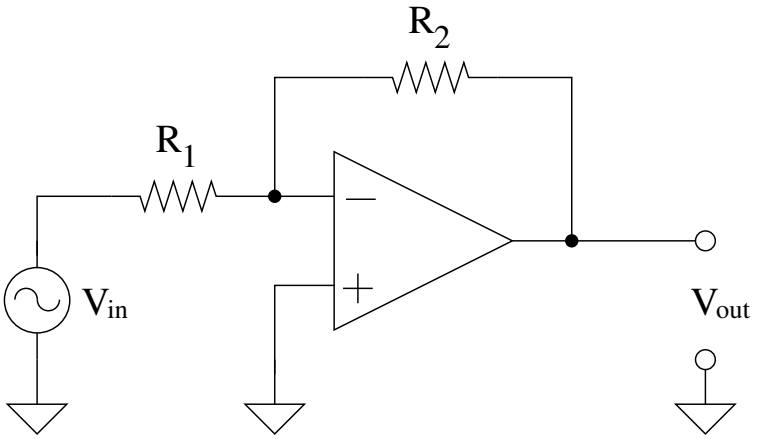


Figure 4: Inverting amplifier for testing the gain-bandwidth product/ slew rate limitations.

(a) Construct an inverting amplifier with unity gain and an input impedance of 1 kΩ (*i.e.* $R_1 =$ 1 kΩ), so as not to "load" the function generator, whose output impedance is 50 Ω. Input a square-wave to see if the output-slope is consistent with your previous finding from the slew rate measurement at unity gain.

(b) At several different frequencies f, input a sine-wave signal. Simultaneously observe the input and output waveforms on your scope, measuring the gain. You should observe two frequency regimes, one where the gain is maintained at a single "plateau" value and one where the gain "rolls off." Take data in both of these frequency regimes and plot your results as gain (in dB) vs. f. Make sure your amplitude at low frequencies is large enough so that you can accurately measure the gain's frequency dependence. Looking at the datasheet, you'll find that the gain-frequency plot is a log-log plot (or semi-log for gain in dB). Before taking data, think about at what frequencies you should measure to get maximum information with a few data points (10 points are typically sufficient).

(c) Repeat the above procedure [(a) and (b)] with an amplifier gain of 100 (which corresponds to 40 dB). Take care to choose an appropriate peak-to-peak input amplitude so that the output of this high-gain amplifier is not forced into saturation.

Questions to think about:

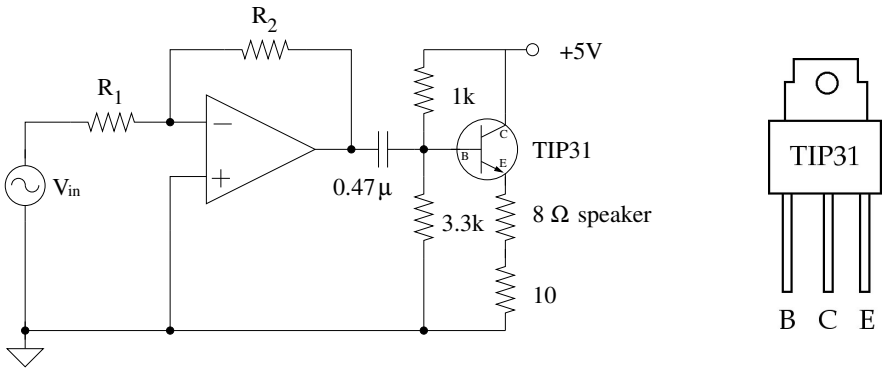
- You should find that the slope of the output waveform for the high-gain amplifier (×100) is smaller than in the unity gain case. Can you explain why?
- For both (b) and (c): What determines the gain, the limited slew rate or the limited gain-bandwidth product? That is, you should compare the frequency dependent gain from (b) and (c) to theory. Ideally you should plot all relevant data on a plot showing gain (in dB) vs. frequency (log scale) and include in your plot(s) lines that show the theoretically expected roll-off. (The typical gain-bandwidth product for the 411 is given in the datasheet).

Optional Lab/ Extracurricular suggestions

For those of you who finish early, you have the opportunity to explore for extra credit two more topics that will become important later in the course. In the first experiment you learn how to boost the output current of operational amplifiers using a power-transistor. In the second experiment you'll learn a nifty way to create a constant current source by using an operational amplifier to stably bias a transistor.

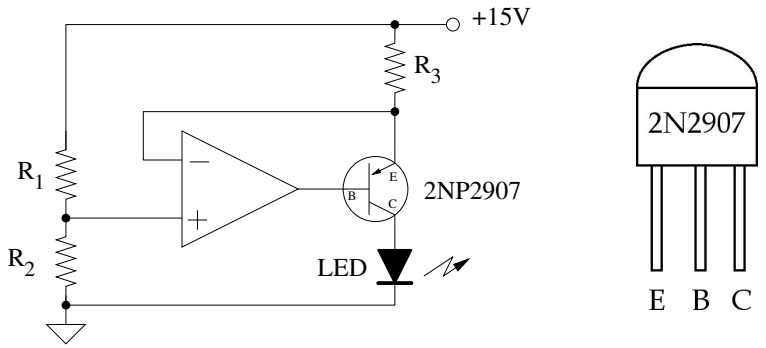
OL1 Current Limit

Try hooking an 8Ω speaker to the output of the circuit in Fig. 4. Is the LF411 capable of providing enough current to drive this small impedance load? Try adding a power transistor to the output as shown below to see if this improves your circuit. Simultaneously measure the speaker voltage on your scope. What happens if you turn up the input voltage too high? Can you hear it?



OL2 Constant Current Source

Choose appropriate values for R_1, R_2, and R_3 in the circuit below so that a constant current of 7.5 mA will flow through the LED. Construct this circuit and verify that a 7.5 mA current is indeed flowing through the LED. How can you halve this LED current by changing just a single resistor? Try it!



References

[1] P. Horowitz and W. Hill, *The Art of Electronics* Cambridge University Press, New York, 1980), pp. 193-194.

National Semiconductor

February 1995

LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

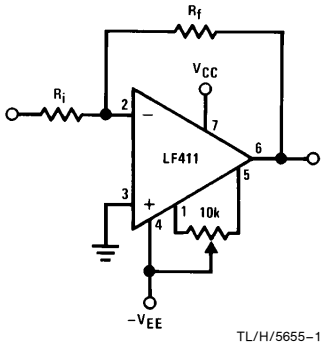
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	0.5 mV(max)
■ Input offset voltage drift	10 μV/°C(max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/$\sqrt{\text{Hz}}$
■ Wide gain bandwidth	3 MHz(min)
■ High slew rate	10V/μs(min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz − 20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



TL/H/5655–1

Ordering Information

LF411XYZ

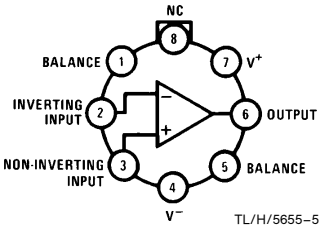
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



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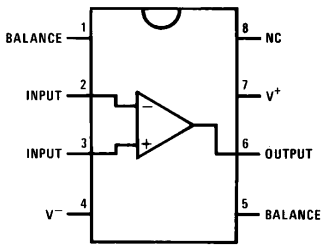
Top View

Note: Pin 4 connected to case.

Order Number LF411ACH or LF411MH/883*
See NS Package Number H08A

Dual-In-Line Package



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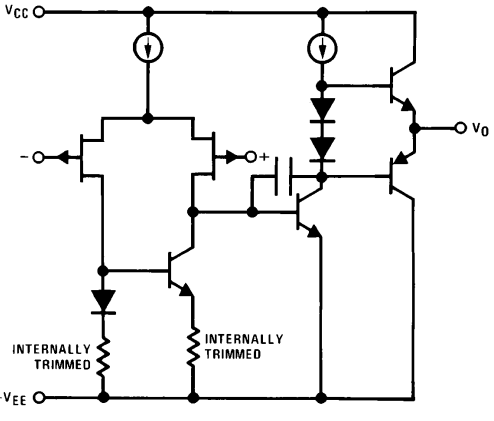
Top View
Order Number LF411ACN, LF411CN or LF411MJ/883*
See NS Package Number N08E or J08A

Simplified Schematic



TL/H/5655–6

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*Available per JM38510/11904

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 2 and 9)	670 mW	670 mW
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 3)	(Note 3)
Storage Temp. Range	$-65°C \le T_A \le 150°C$	$-65°C \le T_A \le 150°C$
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance		Rating to be determined.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S = 10\ k\Omega$, $T_A = 25°C$			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10\ k\Omega$ (Note 5)			7	10		7	20 (Note 5)	μV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		25	100		25	100	pA
			$T_j = 70°C$			2			2	nA
			$T_j = 125°C$			25			25	nA
I_B	Input Bias Current	$V_S = \pm 15V$ (Notes 4, 6)	$T_j = 25°C$		50	200		50	200	pA
			$T_j = 70°C$			4			4	nA
			$T_j = 125°C$			50			50	nA
R_{IN}	Input Resistance	$T_j = 25°C$			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k$, $T_A = 25°C$		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10k$		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	$V_S = \pm 15V$, $T_A = 25°C$	10	15		8	15		V/μs
GBW	Gain-Bandwidth Product	$V_S = \pm 15V$, $T_A = 25°C$	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	$T_A = 25°C$, $R_S = 100\Omega$, f = 1 kHz		25			25		nV/√Hz
i_n	Equivalent Input Noise Current	$T_A = 25°C$, f = 1 kHz		0.01			0.01		pA/√Hz

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of $\theta_j A$.

Note 3: These devices are available in both the commercial temperature range $0°C \leq T_A \leq 70°C$ and the military temperature range $-55°C \leq T_A \leq 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

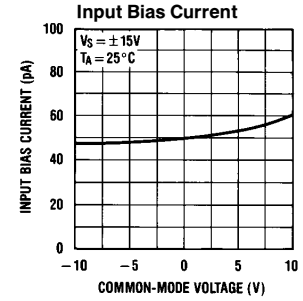
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15V$ to $\pm 5V$ for the LF411 and from $\pm 20V$ to $\pm 5V$ for the LF411A.

Note 8: RETS 411X for LF411MH and LF411MJ military specifications.

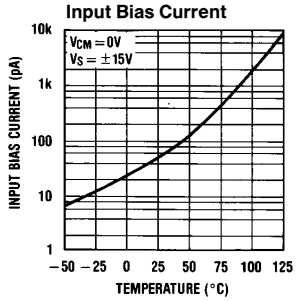
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

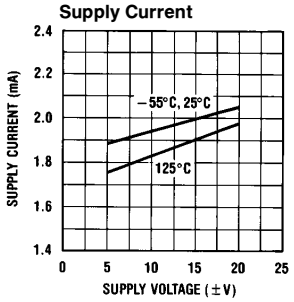
Input Bias Current



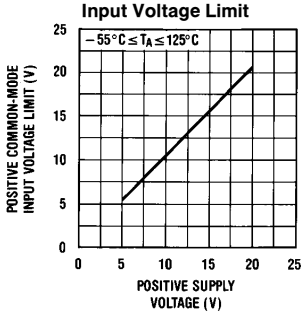
Input Bias Current



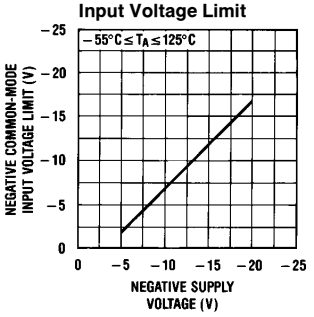
Supply Current



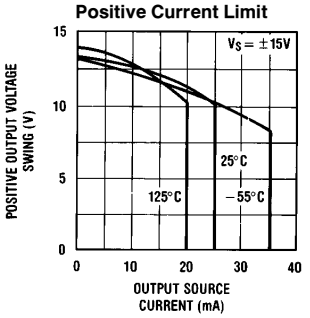
Positive Common-Mode Input Voltage Limit



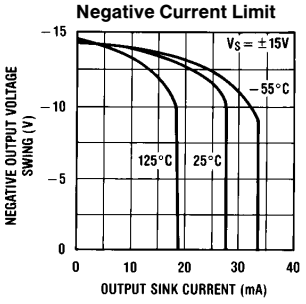
Negative Common-Mode Input Voltage Limit



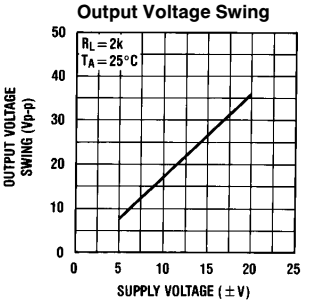
Positive Current Limit



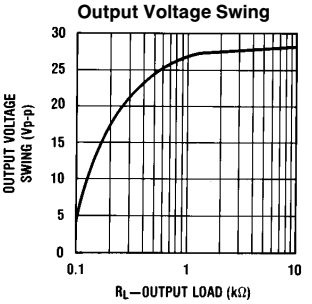
Negative Current Limit



Output Voltage Swing



Output Voltage Swing



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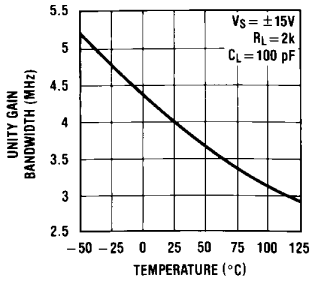
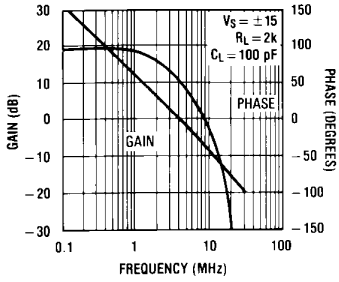
Typical Performance Characteristics (Continued)

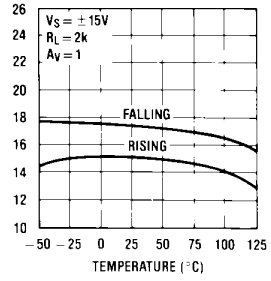
Gain Bandwidth



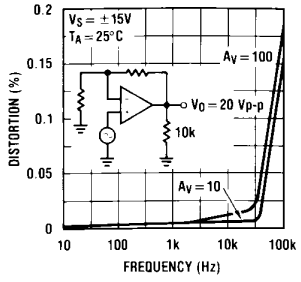
Bode Plot



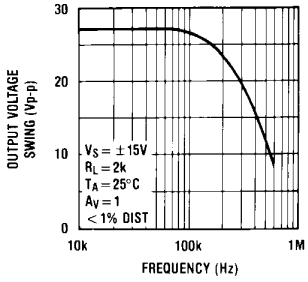
Slew Rate



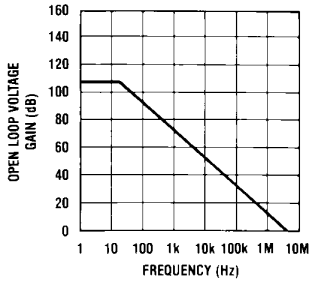
Distortion vs Frequency



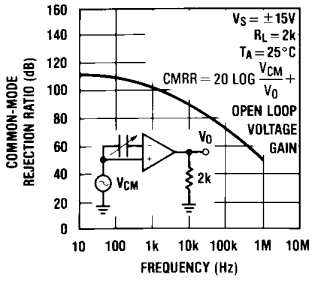
Undistorted Output Voltage Swing



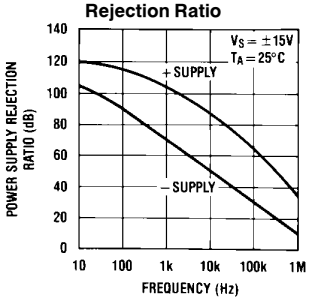
Open Loop Frequency Response



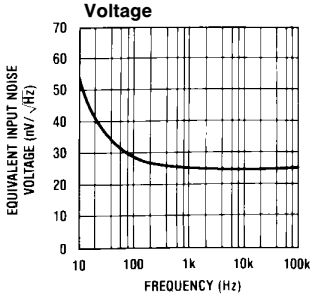
Common-Mode Rejection Ratio



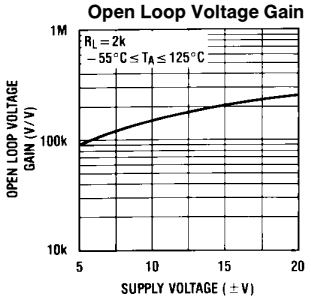
Power Supply Rejection Ratio



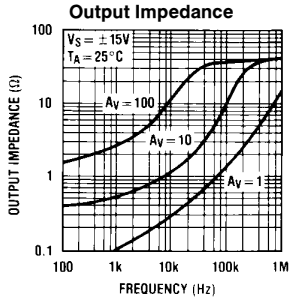
Equivalent Input Noise Voltage



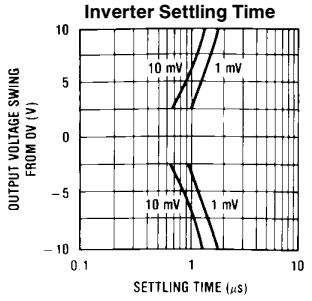
Open Loop Voltage Gain



Output Impedance



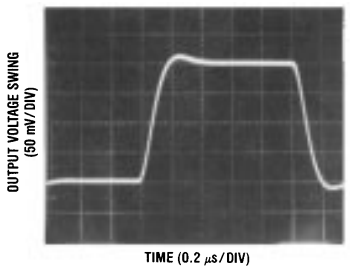
Inverter Settling Time



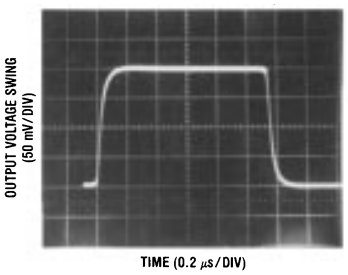
TL/H/5655–3

Pulse Response $R_L = 2\ k\Omega$, C_L 10 pF

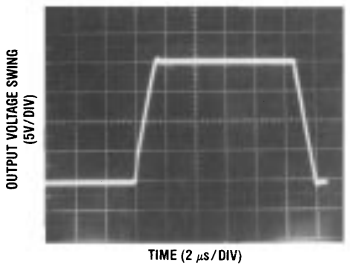
Small Signal Inverting



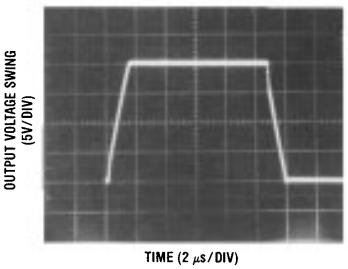
Small Signal Non-Inverting



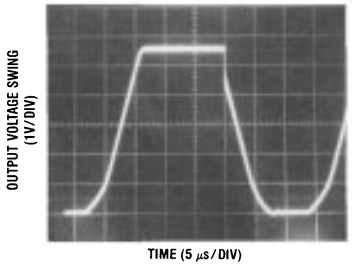
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



TL/H/5655–4

Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

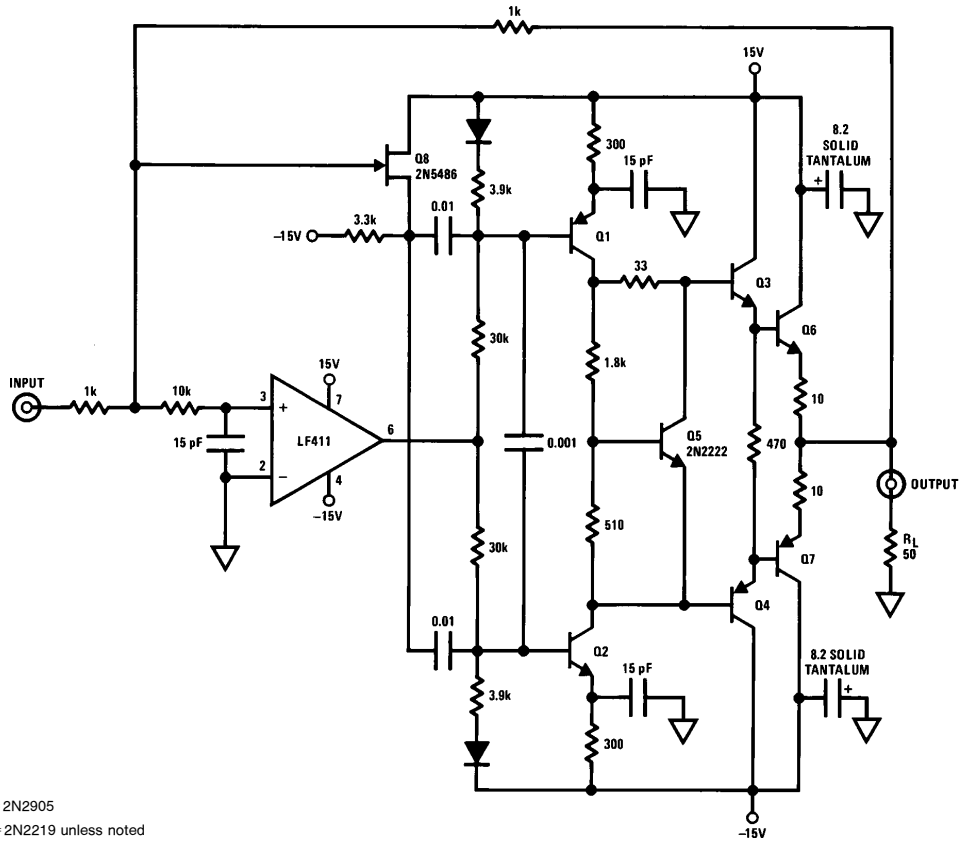
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize ''pick-up'' and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster



PNP = 2N2905
NPN = 2N2219 unless noted
TO-5 heat sinks for Q6-Q7

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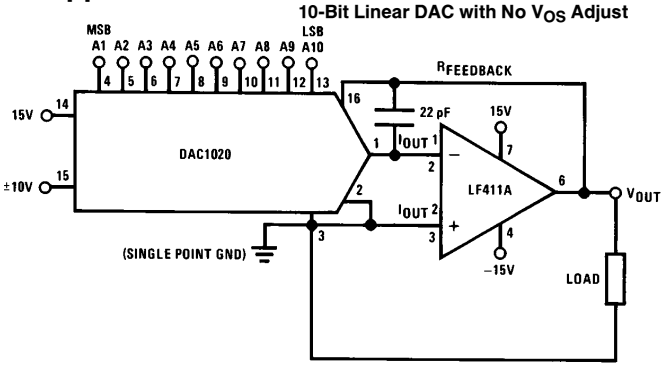
Typical Applications (Continued)

10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

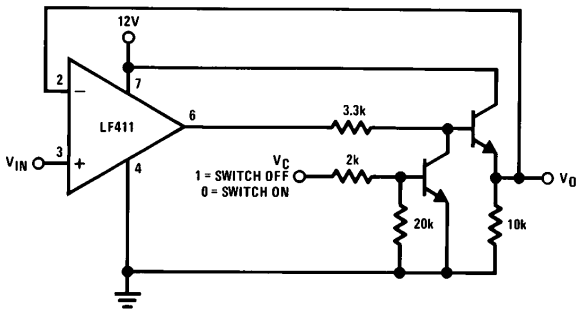
$-10V \le V_{REF} \le 10V$

$$0 \le V_{OUT} \le -\frac{1023}{1024} V_{REF}$$

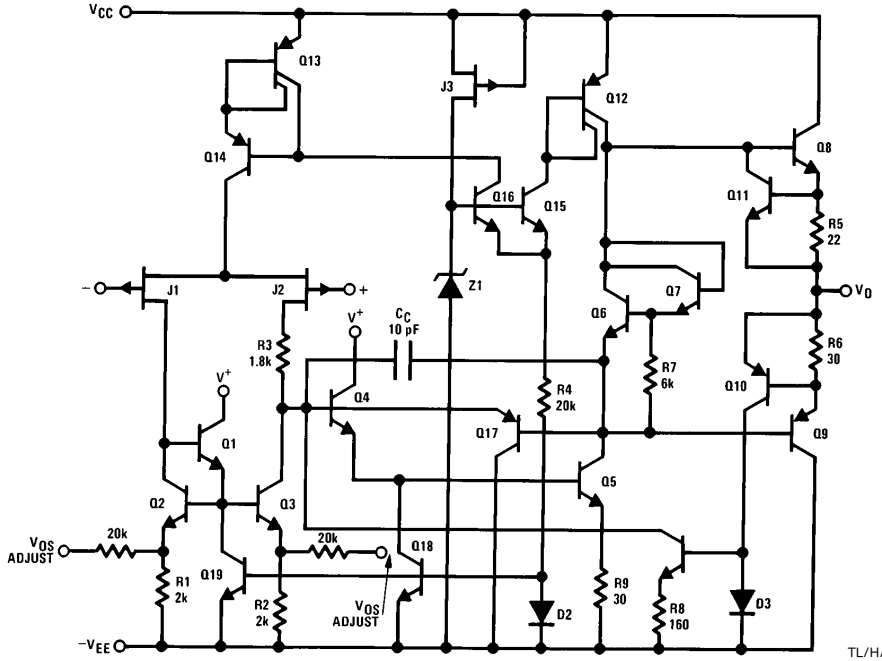
where $A_N = 1$ if the A_N digital input is high

$A_N = 0$ if the A_N digital input is low

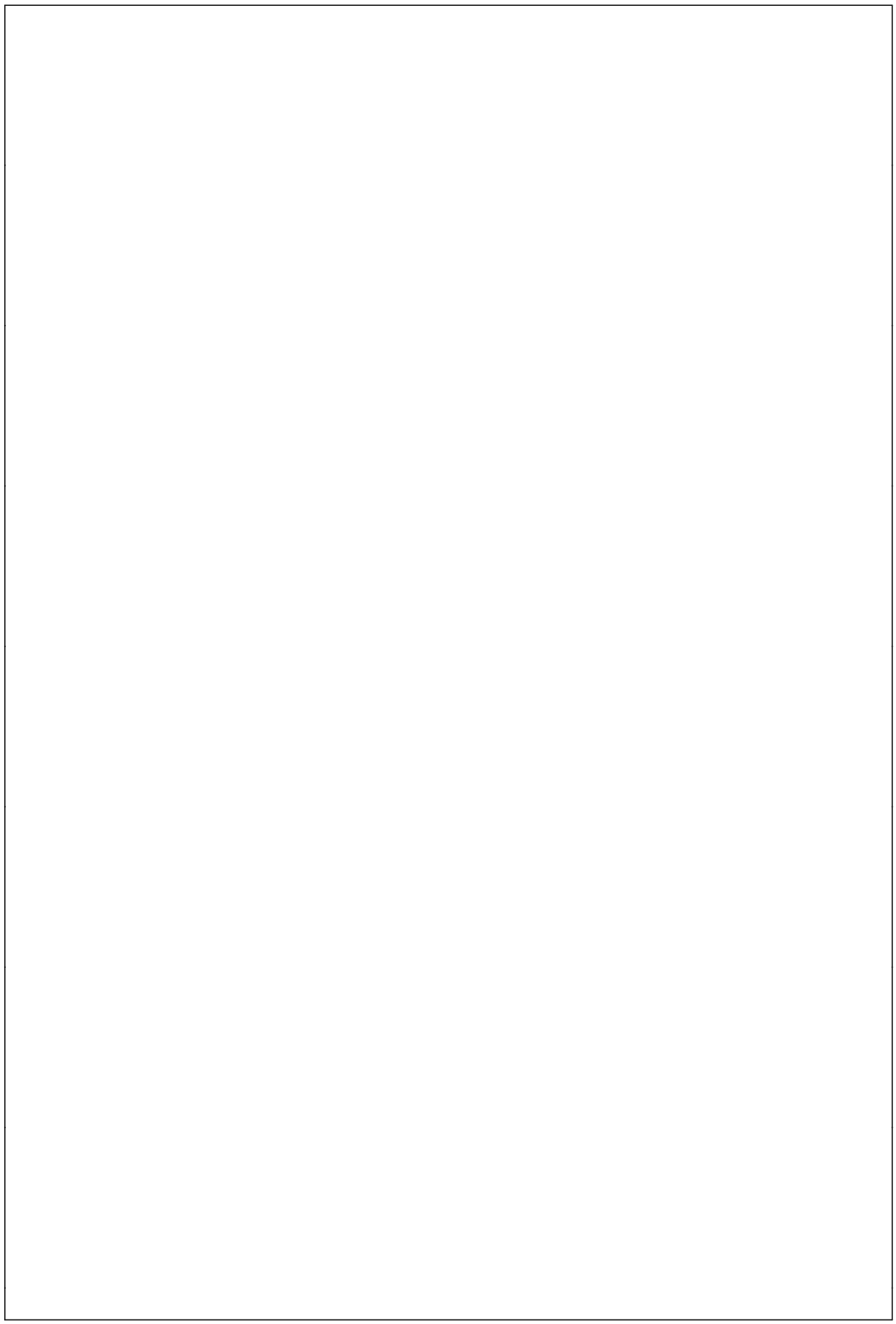
Single Supply Analog Switch with Buffered Output



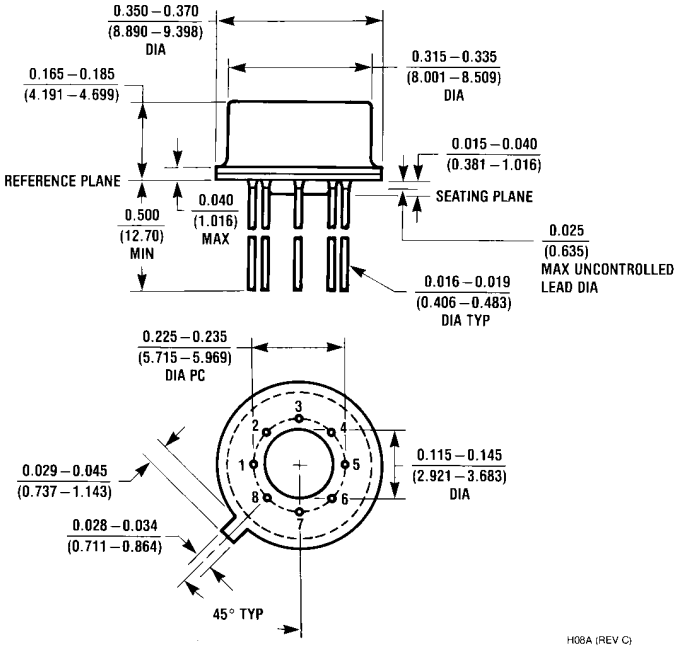
Detailed Schematic



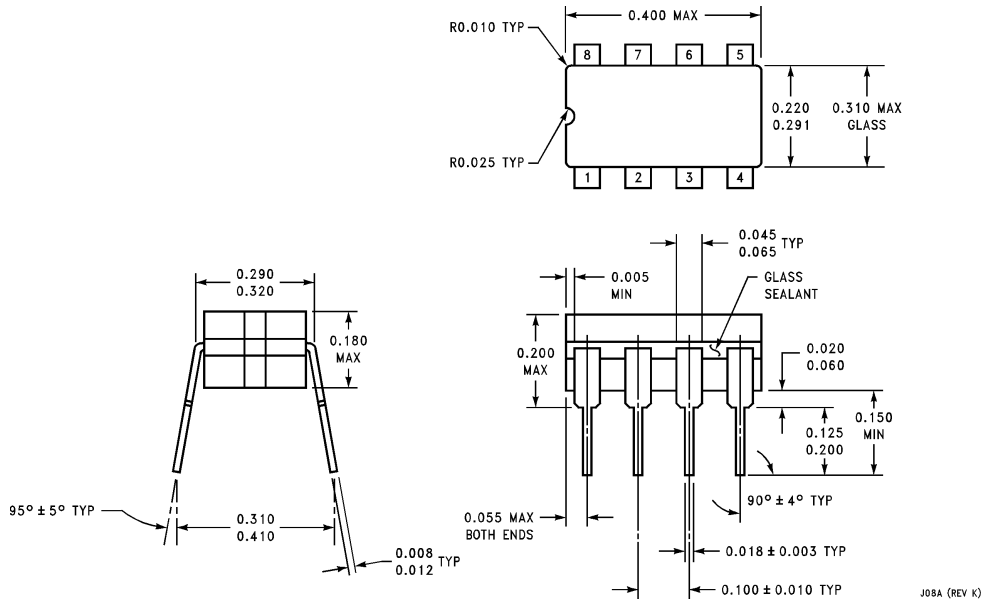
TL/H/5655–10



Physical Dimensions inches (millimeters)

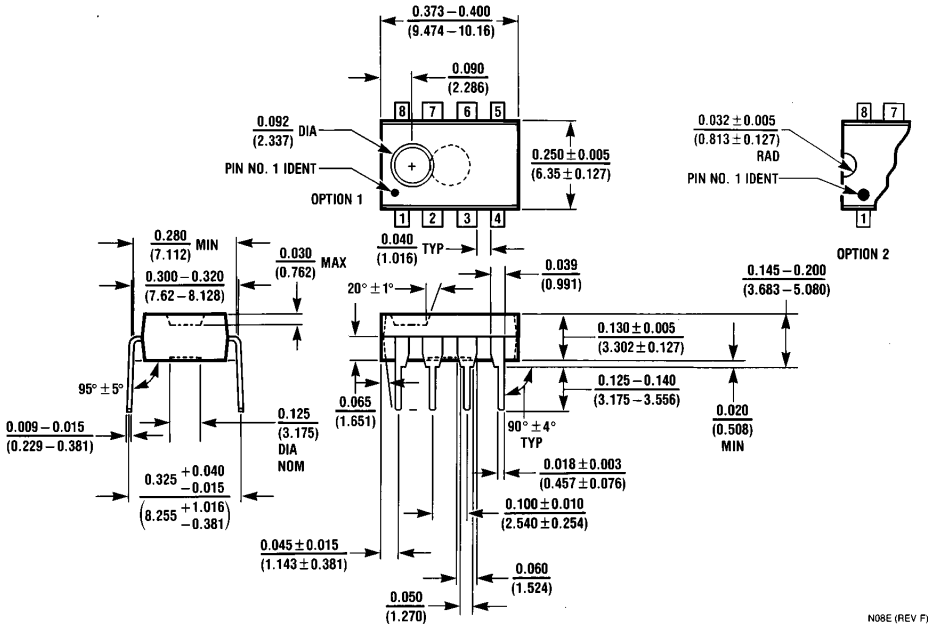


Metal Can Package (H)
Order Number LF411MH/883 or LF411ACH
NS Package Number H08A



Ceramic Dual-In-Line Package (J)
Order Number LF411MJ/883
NS Package Number J08A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LF411ACN or LF411CN
NS Package Number N08E

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