LABORATORY VI : Flip-Flops

Reading: Simpson   Sect. 12.1 - 12.5, 12.8.6 - 12.8.7
                                           Sect. 13.1 - 13.5

Optional reading: Horowitz & Hill   Sect. 8.01 - 8.03, 8.16 - 8.18.

1   Introduction

In this lab we will explore some digital electronics focusing especially on flip-flop circuits. A flip-flop circuit is a binary memory element and forms the basic building block for many memory systems, counters, and other sequential logic circuits, *i.e.* circuits that respond to a series of inputs rather than merely the present input. A flip-flop has two output terminals and two stable voltage states. When operating correctly, if one of the output terminals is in a high voltage state the other output terminal is in a low voltage state. The output voltages of the two terminals can be flipped (exchanged) very quickly by applying a single input pulse to an appropriate input terminal. The new "flipped" state of the output terminals is then stable, *i.e.* it persists even after the input pulse has ended.

2   Laboratory Preliminaries

2.1   Lighting LEDs

In the following lab exercise we will be monitoring the output state of our logical devices using light-emitting diodes (LEDs).
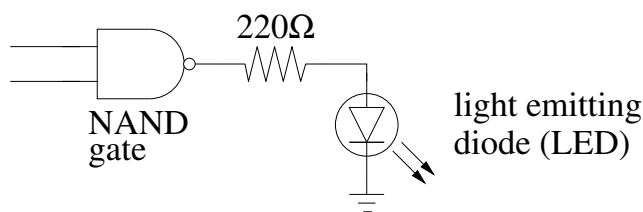

Figure 1: NAND output monitored using an LED

An example is shown to the left, where we monitor the output of a NAND gate. The LED will be lit (dark) when the output is in the high (low) state. The 220 Ω resistor in series with the LED controls the current that is drawn from the NAND gate output and, therefore, the LED brightness. A few tens of milliamps is usually adequate and will not harm the output transistors of the 74LS chips (TTL logic) we will be studying.

On the right hand side of your breadboard there are pre-installed eight LEDs, labeled LED 0 through LED 7, each already connected in series with its own 220 Ω resistor. For example, to construct the above circuit, you would only need to attach the NAND gate's output to the LED 0 input on the lower right-hand side of your breadboard.

If you prefer, there are LEDs available in colors other than green and you may use them instead. The "low port" of the light emitting diodes can be recognized by having a flat part on the plastic housing and also a shorter pin (when new). That is, when building the circuit ground should be

connected to the shorter of the two LED pins and then the flat part will point to ground. This ensures forward bias of the LED and it will light up.

2.2   Handling ICs

Remember to always turn off the power on your breadboard before installing or removing an integrated circuit (IC). Also, please use the available tools to install and remove the IC circuits. Doing this by hand will very often bend the pins.

3   Lab Exercises

3.1   NAND gate Logic

a) Connect a 74LS00 four two-input NAND gate to power (see Fig. 2) and verify for one of the gates that it obeys the NAND truth table. To do so, attach the output to an LED and the inputs to either 0V or +5V.

b) Connect several NAND gates together to make an OR gate and verify its correct operation, *i.e.*, determine the truth table.
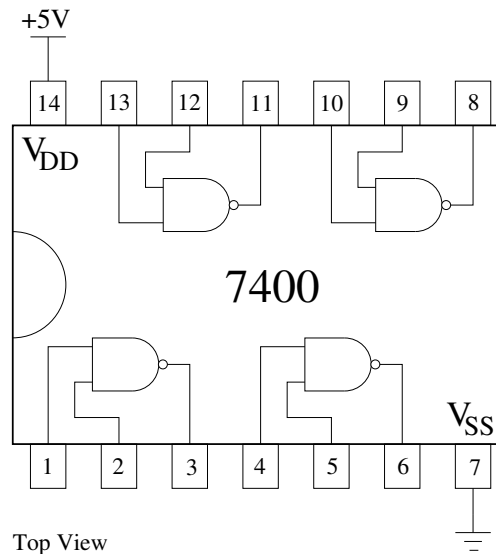

Figure 2: Quad 2-Input NAND gate

3.2   Set-Reset Flip-Flop

Build the set-reset flip-flop shown in Fig. 3a. As indicated in the figure, the inputs to this circuit, labeled $\bar{S}$ and $\bar{R}$, are *active low*, meaning that a change of the output Q results from switching the input from high (+5 V) to low (0 V).

Investigate the properties of the SR flip-flop by testing a variety of input sequences and noting the results.

a) Start with both inputs in the high state. What is Q and $\bar{Q}$? Leave $\bar{R}$ high, take $\bar{S}$ to the low state and back to high. What happens to Q and $\bar{Q}$? Repeat this operation several times.

b) Now leave $\bar{S}$ high, take $\bar{R}$ to the low state and back to high. What happens to Q and $\bar{Q}$?

c) Try various other input sequences and summarize your observation.

d) Try grounding both inputs of the flip-flop, then returning them simultaneously to high. What happens? (This input state is never used and is called indeterminate)
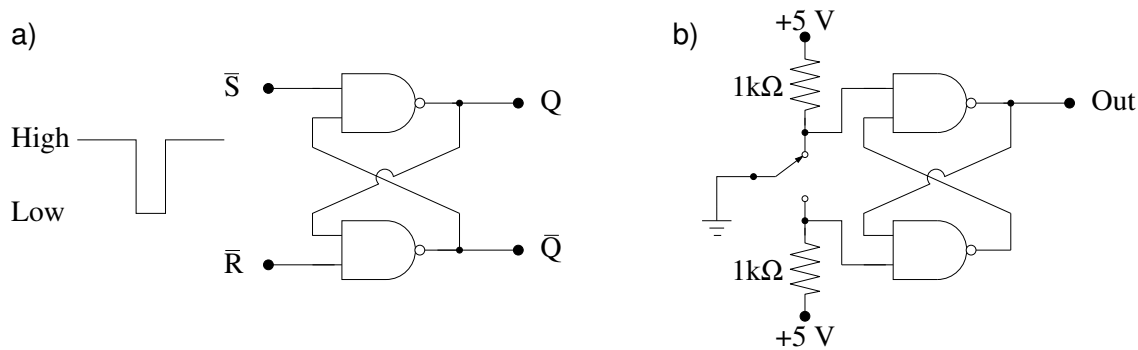

Figure 3: a) Set-Reset Flip-Flop b) NAND debounced switch

3.3   Switch Debouncing using a Flip-Flop

An important application of flip-flops is as "debouncers" for switches. A NAND based debouncer is shown in Fig. 3b. Build this circuit and show that it works as you expect. (Can you explain how it works? Is the switching clean? Is it fast?)

Don't take the circuit apart, we'll need it for the next exercise.

3.4   Divide-by-Two with D Flip-Flop

The 74LS74 circuit, shown in Fig. 4, contains two independent positive-edge clocked D flip-flops. In these flip-flop circuits, the data input at D is passed to the output Q (and as inverted signal to the complement $\bar{Q}$) whenever the clock signal at CLK makes a transition from low to high. Thus Q only changes when CLK makes a positive transition. For normal operation the SET and CLR inputs must be held high.

a) Connect the output of the debounced switch to the clock input CLK, as shown in Fig. 5a. Verify (and report) that the input state of D, for both low and high inputs, can be passed only for positive
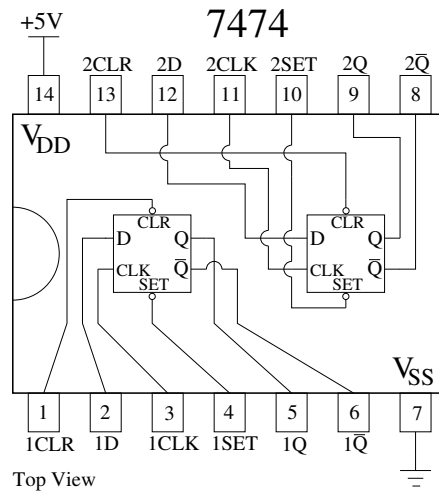
Figure 4: 74LS74: Dual D Edge-Triggered Flip-Flop

going clock signals. Is $\bar{Q}$ the complement of Q?

b) Make a divide-by-two circuit as shown in Fig. 5b. Using the debounced switch check the operation. Does it work as expected? Now, disconnect the debounced switch from the clock and drive the clock with the "sync out" square wave from your signal generator at about 10 kHz. Observe the clock signal and the output simultaneously on the scope.

c) Make a divide-by-four circuit by appropriately wiring two D-flip-flops. Demonstrate that your circuit works. To explain how the final output at one-fourth the input frequency is produced, record one-by-one the input signals and output signals and use these observations to sketch a "timing diagram" (for an example see Simpson pg. 625) .

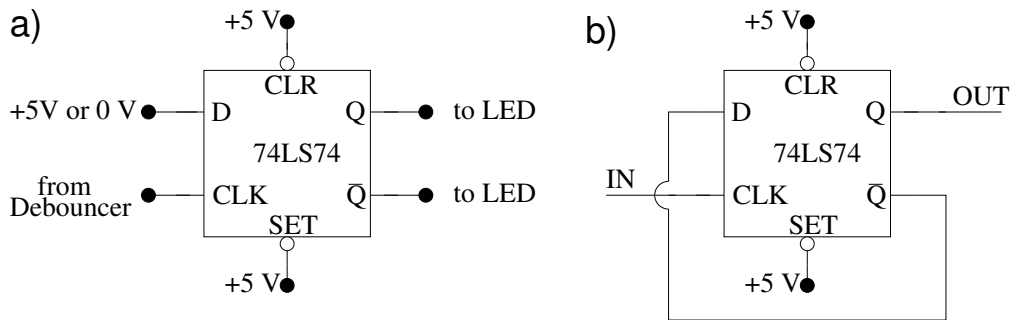Don't take the circuit apart, we'll need it for the next exercise.

Figure 5: a) Set-Reset to test 74LS74 Flip-Flop b) Divide-by-Two with D Flip-Flop

3.5 Multiplexers

A *multiplexer* is the electrical analog of a rotary mechanical switch. It allows one to select one of several input lines and connect it to the output. A *demultiplexer* does the reverse, it allows one to route an input to one of many output lines. Digital electrical multiplexers are unidirectional and one has to buy different IC chips for multiplexing and demultiplexing or purchase integrated chips with both capabilities. These latter IC chips are also simply called multiplexers. Such circuits are essential in many applications. For example in digital communication applications, the data that is to be transmitted is often represented by eight bits (= "byte") and it needs to be send over a single wire, *i.e.* the byte must be sent one-bit at a time. This general problem is called parallel-to-serial conversion and is solved electronically by a multiplexer.

There are also analog electrical multiplexer, which are typically bidirectional, allowing current flow in either direction. In this lab you will explore the operation of the 4051 analog electrical multiplexer (analog MUX). The 4051 is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input (see Fig. 6). The three binary signals (A, B, C) select 1 of 8 channels to be turned on, and connect one of the 8 outputs to the input.
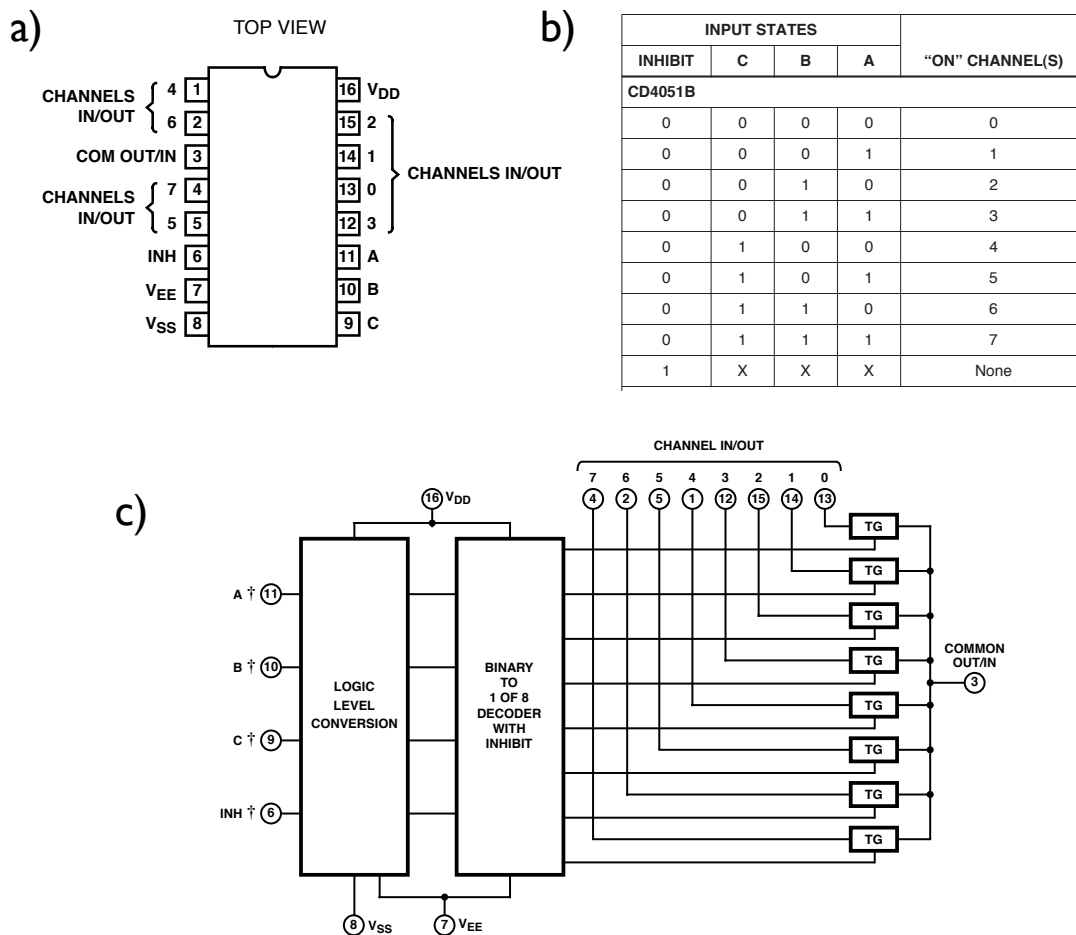

Figure 6: The 4051 analog multiplexer: a) pinout diagram, b) truthtable, c) function block diagram. (Adapted from 4051 datasheet [1])

Control of analog signals up to 20 V_{pp} can be achieved by digital signals, if the digital signal amplitudes are at least 4.5V. More precisely, if the digital supply voltage range is larger 4.5 V ($V_{DD} - V_{SS} > 4.5$ V), then analog output swings are possible with amplitudes set by the supply voltage range $V_{DD} - V_{EE}$ and $V_{DD} - V_{EE} \leq 20$ V. The advantage of analog multiplexers is that they have a low ON impedance and very low OFF leakage current.

In this lab you will use an analog multiplexer to build a digitally controllable amplifier. This is a very useful circuit because in many measurement applications the gain of the input circuitry has to be adjusted depending on the amplitude of the incoming signal in order avoid clipping of the amplified output signals (oscilloscopes are an example).

a) **On resistance**: Measure the On-resistance of output channel 3 of the 4051 analog MUX.

For a possible approach recall last week's lab, where you determined the on-resistance of the 4066 analog switch. Note that you need to connect V_{DD} to 5V, V_{SS} and Inh to ground, and you need to set the input bits (A, B, C) such that output-channel 3 is selected. You may connect V_{EE} to ground or -15V. Does your result agree with the datasheet?

b) **Analog voltage range**: Connect V_{DD} to 5V and V_{SS}, Inh, and V_{EE} to ground. Pick the input bits (A, B, C) such that output channel 3 is selected. Use a 411 opamp to implement a unity gain buffer. Connect the buffer's output to the "Analog In" channel of the multiplexer and the buffer's input to the function generator (Tektronix CFG 280). For a sinusoidal input wave, measure the multiplexer output (channel 3). What is the output voltage range? Does this agree with you expectations? How can you change your circuit to increase the output voltage range? Do it and quantify the result.

c) **Digital Gain Control**: Rewire the 411 opamp used for the unity gain buffer and build the inverting amplifier with digital gain control shown in Fig. 7. (Note that $V_{EE} = -15$V). Pick the resistances R0-R3 such that gains of one, two, three, and four are achieved. Test your circuit and discuss the result. (Does it work as expected? Are there potential issues with this circuit?)

You may test the circuit, for example, by connecting the MUX's digital-inputs A and B to the input line (CLK) and output line (Q) of the divide-by-two circuit you constructed previously and by observing the amplifier output on the oscilloscope. Make sure you drive the divide-by-two circuit using square-waves with *amplitudes in between 0 and 5 V*. It is recommended that you use the sync-out signal of the signal generator and frequencies of around 100 Hz. Since a TTL gate (divide-by-two circuit) is used to drive a CMOS gate (4051 MUX), difficulties may arise because the 3.5 V TTL output-high is barely high enough for CMOS logic. Therefore it is recommended to use a pull up resistor as shown in Fig. 7 before connecting to the A and B inputs of the CMOS 4051 MUX.

References

[1] *CD4051B datasheet*, Texas Instruments Incorporated, 2000. (Available, for example, from `www.ee.washington.edu/stores/DataSheets/cd4000/cd4051.pdf`.)
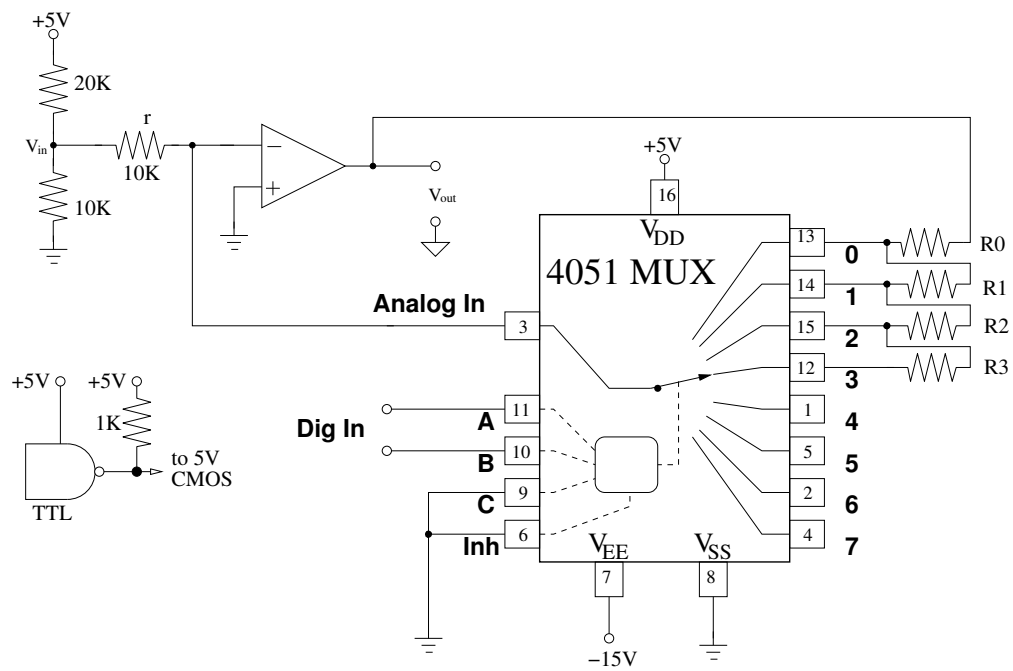
Figure 7: The 4051 analog multiplexer: "rotary control" type schematic of 4051 used to implement an inverting amplifier with digital gain control.